Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claims 1-8 (canceled)

Claim 9 (currently amended): A window ball grid array (WBGA) semiconductor package, comprising:

a core layer having a first surface and an opposite second surface, and a through hole penetrating through the core layer, wherein the second surface is formed with a plurality of wire-bonding portions around the through hole, a plurality of ball-bonding portions, and a plurality of intended-exposing regions around the wire-bonding portions;

at least one chip mounted on the first surface of the core layer and over the through hole, with a portion of the chip exposed via the through hole;

a solder mask layer applied over the second surface of the core layer with the ball-bonding portions being exposed, wherein the solder mask layer is formed with an opening for exposing the through hole, the wire-bonding portions, and the intended-exposing regions;

a plurality of bonding wires which penetrate through the through hole and electrically connect the chip to the wire-bonding portions;

a first encapsulation body formed on the first surface of the core layer for encapsulating the chip;

a second encapsulation body formed on the second surface of the core layer for encapsulating the bonding wires and the intended-exposing regions, wherein a thickness of the second encapsulation body covering the intended-exposing regions is substantially equal to that of the solder mask layer; and

a plurality of solder balls deposited on the ball-bonding portions.

Claim 10 (original): The WBGA semiconductor package of claim 9, wherein a width of the intended-exposing region is of a range from 0.2 to 0.8 mm.

Claim 11 (original): The WBGA semiconductor package of claim 10, wherein the width of the intended-exposing region is 0.4 mm.

Claim 12 (original): The WBGA semiconductor package of claim 9, wherein the intended-exposing regions are located adjacent to the wire-bonding portions.

Claim 13 (original): The WBGA semiconductor package of claim 9, wherein the opening of the solder mask layer is larger in width than a mold cavity of a mold used for forming the second encapsulation body.

Claim 14 (canceled)

Claim 15 (original): The WBGA semiconductor package of claim 9, further comprising: a layer of patterned conductive traces applied between the second surface of the core layer and the solder mask layer.

Claim 16 (original): The WBGA semiconductor package of claim 9, further comprising: another solder mask layer applied between the first surface of the core layer and the chip.

Claim 17 (original): A chip carrier used in a window ball grid array (WBGA) semiconductor package, comprising:

a core layer having a first surface and an opposite second surface, and a through hole penetrating through the core layer;

a conductive trace layer applied over the second surface of the core layer, and formed with a plurality of wire-bonding portions around the through hole, a plurality of ball-bonding portions, and a plurality of intended-exposing regions around the wire-bonding portions; and

a solder mask layer applied over the conductive trace layer with the ball-bonding portions being exposed, and formed with an opening for exposing the through hole, the wire-bonding portions, and the intended-exposing regions.

Claim 18 (original): The chip carrier of claim 17, wherein a width of the intended-exposing region is of a range from 0.2 to 0.8 mm.

Claim 19 (original): The chip carrier of claim 18, wherein the width of the intended-exposing region is 0.4 mm.

Claim 20 (original): The chip carrier of claim 17, further comprising: another solder mask layer applied over the first surface of the core layer.

Claim 21 (new): A chip carrier used in a window ball grid array (WBGA) semiconductor package, comprising:

a core layer having a first surface and an opposite second surface, and a through hole penetrating through the core layer;

a conductive trace layer applied over the second surface of the core layer, and formed with a plurality of wire-bonding portions around the through hole, a plurality of ball-bonding portions, and a plurality of intended-exposing regions around the wire-bonding portions; and

a solder mask layer applied over the conductive trace layer with the ball-bonding portions being exposed, and formed with an opening for exposing the through hole, the wire-bonding portions, and the intended-exposing regions, wherein an encapsulation body in the semiconductor package for covering the intended-exposing regions is substantially equal in thickness to the solder mask layer.

Claim 22 (new): The chip carrier of claim 21, wherein a width of the intended-exposing region is of a range from 0.2 to 0.8 mm.

Claim 23 (new): The chip carrier of claim 22, wherein the width of the intended-exposing region is 0.4 mm.

Claim 24 (new): The chip carrier of claim 21, further comprising: another solder mask layer applied over the first surface of the core layer.